Case Study 1:

1.1)

a.

Yield = 1 + ( defects per unit area x die area))**-N**

die area = 200 mm2 = 2 cm2 , N=14, defects per unit area = 0.04

Yield = 1 + (0.04 x 2)**-14**

= 0.34

b.

Here are the reasons that phoenix have higher defect rate than BlueDragon:

* Phoenix has bigger die size than BlueDragon.
* Phoenix uses more transistors than BlueDragon.
* Phoenix uses more cores than BlueDragon.

1.2)

a.

Phoenix:

From 1.1) a we get Yield of Phoenix = 0.34

Dies per wafer = (Pi x radius**2)/** chip size – ((Pi x diameter)/sqrt(2xchip size))

= (3.14 x 22.5 **2**)/2 – ((3.14 x 45)/sqrt(2x2))

= 794.81 – 70.65

= 724

Profit per chip is $30

Profit = Die Yield x Profit per defect free chip

= 0.34 x 724 x 30

= $7384.8

b.

RedDragon:

Yield = 1 + ( defects per unit area x die area))**-N**

= 1 + (0.04 x 1.2)**-14**

Dies per wafer = (Pi x radius**2)/** chip size – ((Pi x diameter)/sqrt(2xchip size))

= (3.14 x 22.5 **2**)/1.2 – ((3.14 x 45)/sqrt(2x1.2))

= 1233

Profit per chip is $15

Profit = Die Yield x Profit per defect free chip

= 1 + (0.04 x 1.2)**-14 x** 1233 x 15

= $9593.93

c.

Phoenix Die per wafer = 724

RedDragon Die per wafer = 1233

Demand of RedDragon = 50000

Required RedDragon= 50000/1233

= 40.55

Demand of Phoenix = 25000

Required Phoenix = 25000/724

= 34.53

1.3)

a.

Yield = 1 + (0.04 x 0.25)**-14**

~0.87

Probability = Total possible combination x (0.87)**x** x (1-0.87)**8-x**

|  |  |  |
| --- | --- | --- |
| Defect free cores | Possible combinations | Probability |
| 8 | 1 | 0.32821 |
| 7 | 8 | 0.39234 |
| 6 | 28 | 0.20519 |
| 5 | 56 | 0.06132 |
| 4 | 70 | 0.01145 |
| 3 | 56 | 0.00136 |
| 2 | 28 | 0.00010 |
| 1 | 8 | 0.000004 |
| 0 | 1 | 0.00000008 |

Yield for Phoenix**4** = 0.39234 + 0.20519 +0.06132 + 0.01145

= 0.6703

Yield for Phoenix**2** = 0.00136 + 0.00010

= 0.00146

Yield for Phoenix**1** =0.000004

b.

Yield for Phoenix**4** = 0.39234 + 0.20519 +0.06132 + 0.01145

= 0.6703

Yield for Phoenix**2** = 0.00136 + 0.00010

= 0.00146

Yield for Phoenix**1** =0.000004

So, Phoenix**4** has the higher yield than both the other chips so Phoenix**4** being defect free is highly possible. So Phoenix**4** is worthwhile to sell than two other chips.

Case Study 2:

1.4)

a.

Core uses 0.5 watts and there are 4 cores so, total power = 4 x 0.5 = 2 Watts

E**old** = 2T where task operates 8 times faster.

Quad core only operates for only 1/8th of the time and rest it is idle

So energy consumption E**new** = 2 x T/8

= E**old** /8

So, energy consumtion is reduced by 1/8th time for the full power

Power is measured as the rest of consumption of energy at any instant. And energy consumption remains same while the core is running so power doesn’t change and remains same.

b.

New dynamic energy

k x Cl x (V/8)**2** = k x Cl x (V**2**/64)

E**dy, new /** E**dy, old** = k x Cl x (V**2**/64) / (k x Cl x V**2**)

= 1/64

= 0.0156

E**dy, new** = 0.0156 x E**dy, old**

New dynamic power

k x Cl x (V/8)**2**x (F/8) = k x Cl x V**2** x ( F / 512)

P**dy, new /** P**dy, old** = k x Cl x V**2** x ( F / 512) / k x Cl x V**2** x F

= 1/512

= 0.0019

P**dy, new** = 0.0019 x P**dy, old**

c.

Voltage cannot be reduced below 50% of the original voltage.

Voltage can go below upto V/2. New frequency can go below F/8.

Dynamic energy relations,

E**new /** E**old** = k x Cl x (V/2)**2**/ (k x Cl x V**2**)

=V**2 /**4 /V**2**

E**new** = E**old/**4

= 0.25 x E**old**

Power relations,

P**new /** P**old** = k x Cl x (V/2)**2** x (F/8)/ (k x Cl x V**2** x F)

= 1/32

P**new** = 0.0312 x P**old**

Power savings 3.12%.

1.5)

a.

Overall speed up = ( 1 – Fraction**enhanced** + Fraction**enhanced** / Speedup**enhanced**)

Fraction**enhanced**=0.8 since 80% is parallelizable.

Speedup**enhanced**=4

Overall speed up = (1 +0.8+(0.8/4))**-1**

= 2.5

b.

4 cores are parellelized and speed up is 2.5.

Energy ratio

E**quad /** E**single** = 4 x (0.4 V)**2** / V**2**

=0.64

Reducton in energy is 64%.

c.

ASICs can perform the computation for 20% of the power when compared to the general purpose processor.

Total consumed energy = (AISC power consumption x number of AISC) +

(Power consumption in cores x number of cores)

= (0.2 x 2) +( 1 x 2)

= 2.4

Dynamic energy = 2.4 /4

= 0.6 joules

Exercise 1.7)

a.

According to Moore's Law, number of transistors accommodated per square inch on chip doublles every two years. The year span is his 10 years from 2025 to 2015. Device scaling will be the number of transistors in 2025 will be

2**10 ∕ 2 =** 2**5**

= 32 times

b.

Electricity increased about 52% each year form 1990s. So in 2003 performance was 6043 times faster.

From 2025 to 2003 years = 22

Performance 2025 = Base Performance x (1 + rate ∕ 100)**years**

= 6043 x (1 + 52 ∕ 100)**22**

~60507823

Exercise 1.10)

a.

Failure in time (FIT) = 10**9**/ Mean time to failure(MTTF)

(MTTF) = 10**9**/100

= 10**7**

b.

The Mean Time To Recovery (MTTR) is 1 day, thus. The previous issue reveals that the Mean Time To Failure (MTTF) is 10 hours.

MTTR = 24 hours

Availibility = MTTF / (MTTF + MTTR)

= 10**7** / (10**7** + 24)

~ 100%

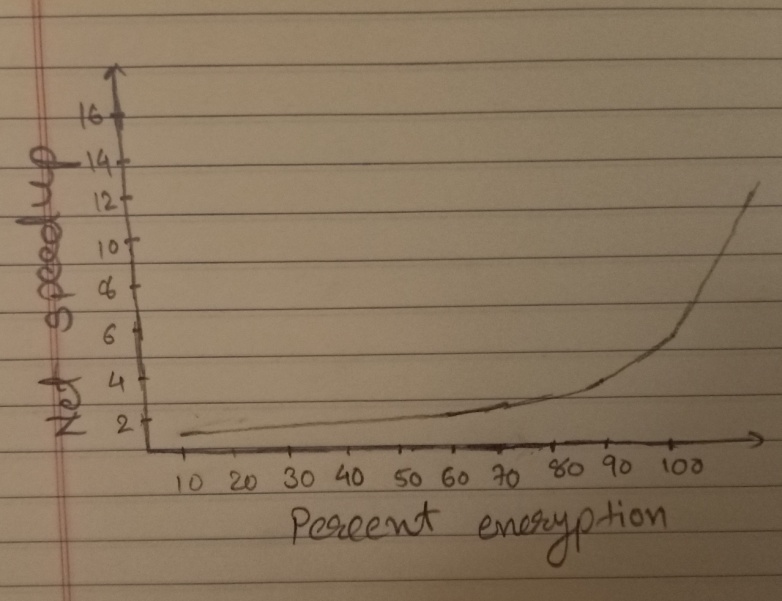
Exercise 1.12)

a.

after enhancing the encryption operation speed up is 20 .

speed up = 100 / ((100 - Fraction**enhanced**) + (Fraction**enhanced**/ Speed up**enhanced**))

= 100 / ((100-x) +(x/20))



b.

speed up equals 2

speed up = 1 / (1 - Fraction**enhanced** + (Fraction**enhanced**/ Speed up**enhanced**))

= 1 / (1- x/100 +(x/20x100))

2 = 1/ (1- 19x/2000)

x = 2000/38

= 52.63%

c.

percentage of encryption with encryption with encryption hardware added to speedup is 52.63%.

(0.526/20)/((1-0.526) + (0.526/20)) = (0.526/20)/((0.474) + (0.526/20))

= 5.25%